CBCS SCHEME

USN | | | | | | | | | | |

15EC555

Fifth Semester B.E. Degree Examination, June/July 2019
MSP430 Microcontroller

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. With a neat block diagram, explain the architecture of MSP430 microcontroller. **(10 Marks)**
b. Mention the features of MSP430. **(06 Marks)**

OR

2 a. With a neat diagram explain the MSP430 memory map structure. **(10 Marks)**
b. Explain the clock generator of MSP430 and also mention the clock ranges of each. **(06 Marks)**

Module-2

3 a. Explain the different addressing Modes of MSP430 and give example. **(10 Marks)**
b. Describe the MSP430 stack operation. **(06 Marks)**

OR

4 a. Explain the following instructions:
i) ADC.W dst ii) SUBC.W Src, dst iii) TST.W dst
iv) DADD.W Src, dst v) BIS.W Src, dst vi) SWPb Src **(12 Marks)**
b. What is the difference between unconditional and conditional jump and mention the working range? **(04 Marks)**

Module-3

5 a. With a neat diagram, explain the MSP430 clock system. **(10 Marks)**
b. Explain the digitally controlled oscillator of MSP430. **(06 Marks)**

OR

6 a. Explain the step involved in the interrupt service Routine of MSP430. **(10 Marks)**
b. Explain the different low power modes of MSP430. **(06 Marks)**

Module-4

7 a. With a neat diagram explain the Comparator_A+ inbuilt module of MSP430. **(08 Marks)**
b. Explain the MSP430 ADC10 Successive approximation ADC. **(08 Marks)**

OR

8 a. Explain the MSP430 digital to Analog conversion. **(06 Marks)**
b. With a neat diagram explain the architecture of Sigma Delta ADC. **(10 Marks)**

Module-5

9 a. Explain the MSP430 Digital input and output parallel ports. **(08 Marks)**
b. Explain the MSP430 serial peripheral interface. **(08 Marks)**

OR

10 a. Explain the MSP430 asynchronous serial communication. **(08 Marks)**
b. Write short note on: i) Universal serial interface ii) Universal serial communication interface. **(08 Marks)**

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